Korean J. Chem. Eng., **25**(2), 373-376 (2008)

Reduction of proximity effect in electron beam lithography by deposition of a thin film of silicon dioxide

Chang-Ho Seo and Kahp-Yang Suh†

School of Mechanical and Aerospace Engineering and the Institute of Bioengineering,
Seoul National University, Seoul 151-742, Korea
(*Received 5 January 2007 • accepted 25 July 2007*)

Abstract−We present a simple strategy to reduce the writing time of electron beam lithography (EBL) by using a highly sensitive Shipley's UV-5 resist while reducing proximity effects by depositing a thin film of silicon dioxide (SiO_2) on silicon substrate. It was found that a simple insertion of a thin SiO_2 film greatly reduced proximity effects, thereby providing enhanced resolution and better pattern fidelity. To support this conclusion, the bottom line width and sidewall slope of the developed pattern were analyzed for each substrate with different film thickness.

Key words: Electron Beam Lithography (EBL), Proximity Effect, Thin Film, Silicon Dioxide

INTRODUCTION

Electron beam (e-beam) lithography (EBL) is regarded as a valuable nanofabrication tool to construct high-resolution patterns for mask-making or direct writing. One of the critical drawbacks of EBL is long exposure time due to its serial patterning characteristic. Until now, EBL has found a wide range of uses in research, but has yet to become a standard technique in industry due to low speed and high cost. Extensive efforts have been made to develop resists with better exposure characteristics including poly(methyl methacrylate) (PMMA) and other chain-scission resists [1]. Consequently, these efforts have given birth to a series of resists with improved sensitivity, resolution, and etching resistance [2]. The widespread use of high sensitivity resists, however, has been limited by proximity effects, resulting in broader bottom line width and poor edge definition.

Although EBL exhibits superior performance in creating minimum feature size, the proximity effect generated from forward and backward scatterings makes it difficult to precisely determine the distribution of electron irradiation [3]. This undesired effect becomes more pronounced in the sub-100-nm regime especially for highly sensitive resists. Several techniques have been proposed to address this problem such as exposure of low energy e-beam [4], computer-aided numerical analysis [5,6], dosage compensation [7,8], multilayer resists coating techniques [9], shape modification [10,11] and insertion of an intermediate layer [12,13].

In this communication, we further expanded the method of a layer insertion by depositing a thin film material with low atomic number (e.g., SiO_2) on bare silicon substrate and evaluated the proximity effect. Since an undercut profile of the resist is typically observed for positive-tone CARs owing to backscattered electrons, it is imperative to consider and devise the effective methods to reduce the undesired proximity effect. This is particularly important when a high sensitivity e-beam resist is used. In this study, the Shipley's UV-5 positive tone CAR (UV-5 hereafter) is tested as a resist material whose sensitivity is about 16 μC/cm^2 at 30 keV, almost 10 times higher than that of PMMA in terms of area dose. This superior sensitivity could reduce long exposure time while compromising pattern fidelity by proximity effects. The motivation of this study is thus to investigate a simple method to reduce proximity effects by depositing a thin film of silicon dioxide for UV-5.

EXPERIMENTAL

A 4-inch silicon wafer (<0.01 Ω) with a thickness of 525 μm was used as bare substrate. The substrate was cleaned in nitric acid, rinsed in deionized (DI) water, placed in buffered HF, and rinsed again for 2 min in a flow stream of DI water. The cleaned wafer was baked at 115 °C for 10 min to remove any residual water. A thin film of SiO_2 was deposited on the substrate by a low pressure chemical vapor deposition reactor (LPCVD, Inter-university Semiconductor Research Center, Seoul National University) with a thickness of 500 Å, 1,000 Å, and 1,500 Å, respectively, using oxygen and tetraethylorthosilicate as reacting gases at a pressure of 1 Torr and a temperature of 675 °C. Hexamethyldisilane (HMDS) was spun onto the wafer at 4,000 rpm for 50 s in order to improve the adhesion of the resist. Then, the UV-5 was spun onto the wafer in the same way to obtain a 400 nm-thick layer. The wafer was then pre-baked on a hot plate at 132 °C for 1 min. After that, the UV-5 resist film was exposed to E-beam at 30 keV using EBMF10.5 system (Leica Microsystems Lithography, Germany - a Gaussian beam machine). The specification of the system is shown in Table 1. The exposed resist was treated with a post-exposure bake (PEB) at 135 °C for 90 s. After the PEB, each wafer with patterned resist was developed with MF CD-26

Table 1. Specification of EBL used in this experiment

Electron source	LaB_6
Acc. voltage	30 keV
Pattern generator	10 MHz
Scanning type	Vector Scan
Working area	1.6384 mm
Beam shape	Gaussian beam

†To whom correspondence should be addressed.
E-mail: sky4u@snu.ac.kr

for 90 s. The developed wafer was rinsed by flowing DI water for 5 min and then the rinsed wafer was hard baked at 112 °C for 2 min.

RESULTS AND DISCUSSION

The relationship between the area dose for sufficient exposure in resist and the demanding exposure time is given by

$$T = \frac{D \times A}{I} \quad (1)$$

where T is the exposure time (second), D is the area dose (C/cm^2), A is the exposure area (cm^2), and I is the beam current (A). According to this formula, a low sensitivity resist (or a huge area dose) needs much dwelling time of the e-beam. Therefore, use of the high sensitivity UV-5 instead of PMMA can reduce exposure time, which in turn gives rise to high throughput. This could be of great benefit when large area patterning is necessary while recognizing that the proximity effect by backscattering is expected to become more pronounced [14].

To evaluate the pattern profile of the UV-5 resist with different thickness of SiO_2, line widths (especially bottom critical dimensions) and sidewall slopes (edge definition) of the resulting resist profiles were measured for each substrate through SEM inspection. Since the proximity effect produces an undercut profile (broader bottom CDs) and thus worsens sidewall edge slope, this simple inspection can serve as an indicator to measure proximity effects. The line widths of the tested patterns were 2 μm, 1 μm, 0.5 μm and 0.3 μm. To produce reliable data, ten samples were measured for each pattern size and then average values were obtained with standard deviation. As shown in Fig. 1, the line that had been written at a dose of 16 μC/cm^2 and with an intensity of 30 keV gradually approached the designed pattern size with vertical slope by increasing the SiO_2 thickness. As a comparison, in the absence of SiO_2 thin film, the largest line width was found with poor edge profile for all pattern sizes. The opposite was observed in the presence of SiO_2 thin film. Fig. 2 shows SEM images of 0.2 μm line-and-space patterns with differ-

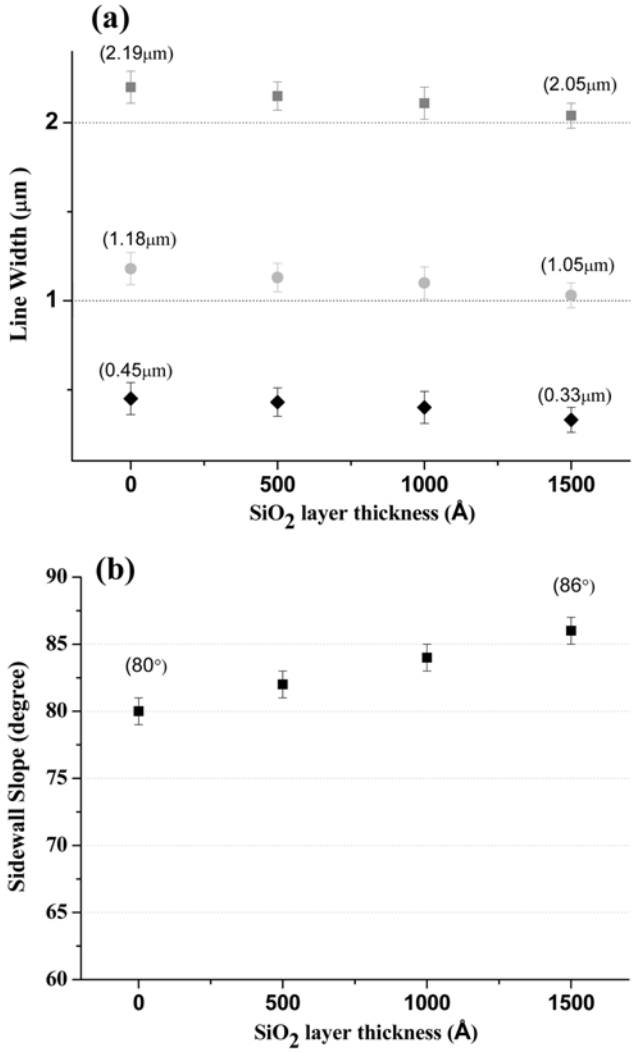

Fig. 1. (a) Plot of the line width and (b) slope of the exposed pattern with different thickness of SiO_2 (500 Å, 1,000 Å, and 1,500 Å). Three line-and-space patterns were used for these plots: 1 μm, 2 μm and 3 μm. The standard deviation in line width ranged from 0.06 to 0.08 μm and ~3° in slope.

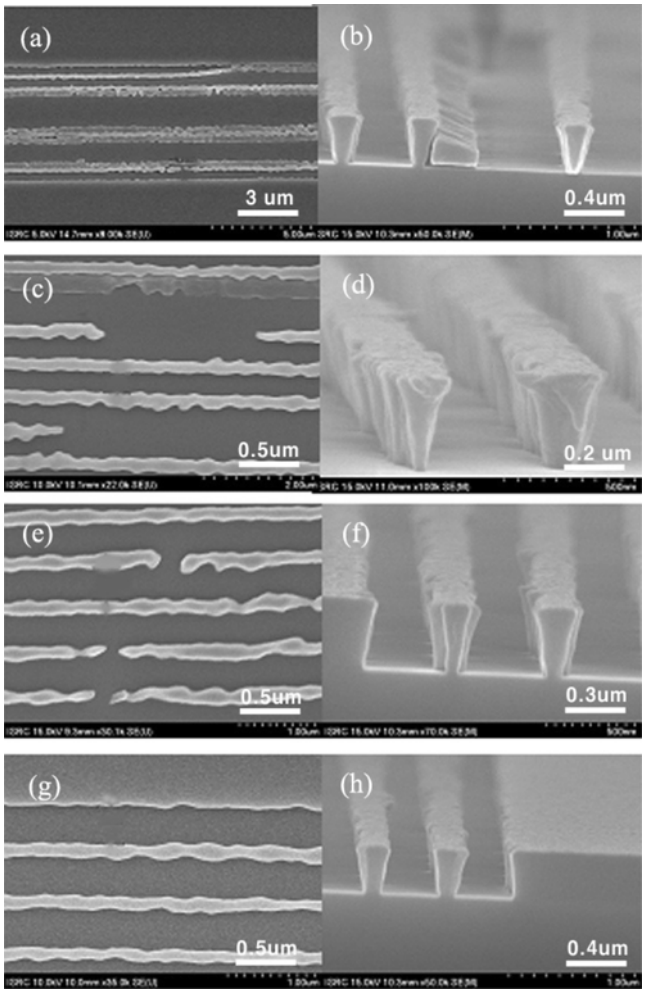

Fig. 2. SEM images showing the fabricated 200 nm lines using EBL: (a-b) bare silicon wafer, (c-h) silicon wafer with a thin film of SiO_2 (500 Å, 1,000 Å, and 1,500 Å from top to bottom). Planar images are shown on the left along with the corresponding cross-sectional images on the right.

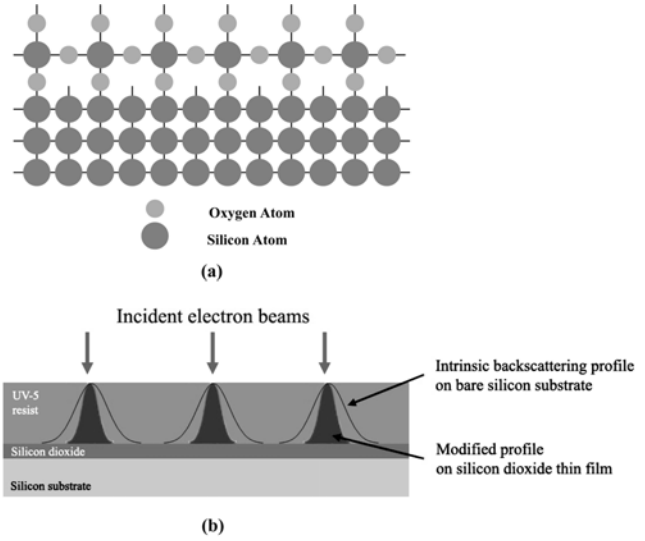

Fig. 3. A schematic diagram for (a) the bonding interface between silicon wafer and SiO_2 thin film and (b) a modified profile of the backscattering electrons on the SiO_2 thin film.

ent SiO_2 film thickness. In the case of bare silicon wafer, several lines were lifted off and the remaining lines were disconnected by the proximity effect as seen from (a-b). However, the patterns on the SiO_2 substrate from (c) to (h) were much improved with increasing the thickness of SiO_2. Of the conditions tested, a thin film with a thickness of 1,500 Å was found to be optimal as judged by the resulting lines without disconnection or lift-off. A further increase of film thickness would result in better performance, but the removal of the sacrificial SiO_2 layer would be additional burden to the whole process. Thus, a higher thickness than 1,500 Å was not tested.

To explain how a thin film of SiO_2 acts as a blocking layer against backscattered electrons, a schematic diagram for the bonding interface of silicon wafer and SiO_2 thin film is shown in Fig. 3(a). In general, scatterings can be divided into forward and backward scatterings. A common polymer resist consists of carbon, hydrogen and oxygen with low atomic number, and thus the density of atoms is quite low. Hence, the entire beam electrons undergo small-angle forward scattering, which makes the diameter of an incident beam broader. The beam diameter (d_f) by forward scattering can be expressed by a simple equation [15]:

$$d_f = 0.9\left(\frac{R_t}{V_b}\right)^{1.5} \quad (2)$$

where R_t is the resist thickness in nanometer and V_b is the beam voltage in kilovolt. Therefore, the forward scattering can be decreased by reducing resist thickness and increasing beam voltage. Also, this forward scattering is dominant mainly when the patterning is performed at a low beam voltage below 10 keV. After electrons pass through the resist onto silicon substrate, some of them undergo large angle Gaussian shape backscattering, which causes additional resist exposure. Since we used a high accelerating voltage (30 keV), backscattering electrons are more influential than forward-scattering electrons in proximity effect. In the presence of oxygen atoms, which are smaller than silicon atoms, the number of backscattered electrons is known to be decreased [12,13]. For example, in the case of 2 μm line pattern, the exposed line width on bare silicon substrate was 2.19 μm on average (~10% deviation), whereas the width was decreased to 2.05 μm on 1,500 Å thick SiO_2 layer (~3% deviation). Furthermore, the slope of the exposed lines on the bare silicon wafer was ~80 degrees, whereas the value was ~86 degrees on 1,500 Å thick SiO_2 layer. The modified profile of the backscattering electrons on the SiO_2 thin film is illustrated in Fig. 3(b). Due to limitations of the e-beam facility used in our experiment (beam diameter ~50 nm), further reduction in feature size was not attempted. Use of a smaller beam size with dimensions less than 100 nm is currently under study in our laboratory to compare with pattern replications in soft or nanoimprint lithography [16].

SUMMARY

We have presented a simple strategy to reduce proximity effects by adding a thin film of SiO_2 on bare silicon substrate. Using this method, we have examined the effects of SiO_2 thickness on the bottom CDs and edge definition after exposure. It was found that the pattern size gradually approached the designed pattern size with vertical wall as the thickness of SiO_2 increased. Of the three thicknesses tested in this experiment (500 Å, 1,000 Å, and 1,500 Å), a higher thickness gave rise to stable line patterns without disconnection or lift-off. A further increase of film thickness would result in better performance, but the removal of the layer would be an additional burden to the whole process.

ACKNOWLEDGMENT

This work was supported by the Grant-in-Aid for Next-Generation New Technology Development Programs from the Korea Ministry of Commerce, Industry and Energy (No. 10030046). This work was also supported in part by the Micro Thermal System Research Center of Seoul National University.

REFERENCES

1. D. R. Medeiros, A. Aviram, C. R. Guarnieri, W. S. Huang, R. Kwong, C. K. Magg, A. P. Mahorowala, W. M. Moreau, K. E. Petrillo and M. Angelopoulos, *IBM Journal of Research and Development*, **45**, 639 (2001).
2. W. M. Moreau, *Semiconductor lithography: principles, practices, and materials*, *microdevices*, Plenum Press, New York, (1988).
3. L. F. Thompson, C. G. Willson and M. J. Bowden, *Introduction to microlithography*, 2nd ed, ACS professional reference book, American Chemical Society, Washington, DC (1994).
4. C. Stebler, M. Despont, U. Staufer, T. H. P. Chang, K. Y. Lee and S. A. Rishton, *Microelectronic Engineering*, **30**, 45 (1996).
5. E. Seo, B. K. Choi and O. Kim, *Microelectronic Engineering*, **53**, 305 (2000).
6. R. Wuest, P. Strasser, M. Jungo, F. Robin, D. Erni and H. Jackel, *Microelectronic Engineering*, **67-8**, 182 (2003).
7. E. H. Anderson, D. L. Olynick, W. L. Chao, B. Harteneck and E. Veklerov, *Journal of Vacuum Science & Technology B*, **19**, 2504 (2001).
8. S. J. Wind, P. D. Gerber and H. Rothuizen, *Journal of Vacuum Science & Technology B*, **16**, 3262 (1998).

9. J. B. Kruger, P. Rissman and M. S. Chang, *Journal of Vacuum Science & Technology*, **19**, 1320 (1981).
10. E. Kratschmer, *Journal of Vacuum Science & Technology*, **19**, 1264 (1981).
11. S. Y. Lee and B. D. Cook, *IEEE Transactions on Semiconductor Manufacturing*, **11**, 108 (1998).
12. E. A. Dobisz, C. R. K. Marrian, R. E. Salvino, M. A. Ancona, F. K. Perkins and N. H. Turner, *Journal of Vacuum Science & Technology B*, **11**, 2733 (1993).
13. C. T. Pan and M. F. Chen, *Nanotechnology*, **16**, 410 (2005).
14. K. Wilder, C. F. Quate, B. Singh and D. F. Kyser, *Journal of Vacuum Science & Technology B*, **16**, 3864 (1998).
15. P. Rai-Choudhury, *Handbook of microlithography, micromachining, and microfabrication*, 2 vols, SPIE Optical Engineering Press, London (1997).
16. K. Y. Suh, H. E. Jeong, J. W. Park, S. H. Lee and J. K. Kim, *Korean J. Chem. Eng.*, **23**, 678 (2006).