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Optimization of single-walled carbon nanotube growth and study of the hysteresis of random network carbon nanotube thin film transistors

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Abstract−Random network single-walled carbon nanotube (SWNT)-based thin film transistors show excellent properties in sensors, electronic circuits, and flexible devices. However, they exhibit a significant amount of hysteresis behavior, which should be solved prior to use in industrial applications. This paper provides optimum conditions for the growth of random network SWNTs and reveals that the observed hysteresis behavior originates from the charge exchange between the SWNTs and the dielectric layer rather than from changes in the intrinsic properties of the SWNTs. This was proven by studying the conditions of stepwise gate sweep experiments and time measurements. This paper also shows that top gate SWNT thin film transistors (TFTs) with an SU-8 dielectric layer could provide a practical solution to the hysteresis problem for SWNT TFTs in electronic circuit applications.

Key words: Single Walled Carbon Nanotubes, Thin Film Transistor, Hysteresis, Catalyst

INTRODUCTION

Single-walled carbon nanotube (SWNT)-based thin film transistors (TFTs) have been widely studied for use in chemical sensors [1,2], optoelectronic devices [3,4], and electronic circuits [5-10], due to the extremely high mobility and sensitivity of SWNTs. The high sensitivity of SWNTs makes them suitable for sensor applications and modification of the electronic properties of SWNT TFTs [11], but this also makes SWNT devices susceptible to hysteresis effects and causes their electronic properties to fluctuate due to the charges moving near the SWNTs during transistor operation. Research has been conducted to study the effects of the surface status of the dielectric layer on the hysteresis [12-14], and various approaches have been reported to prevent the hysteresis behavior, including use of a low operation voltage with a thin organic [15], high k gate dielectric [16] and self-assembled monolayer [17]. This paper provides optimum conditions for the growth of the SWNTs and reports a systematic study of the hysteresis behavior of chemical vapor deposition (CVD) grown random network SWNT TFTs with variations in the gate bias conditions and the TFT channel length. In addition, prevention of the hysteresis through fabrication of the top gate SWNT TFT is shown.

EXPERIMENTAL

Random sub-monolayer networks of SWNTs were first grown onto SiO_2 (100 nm)/Si wafers using established CVD techniques [18]. The general procedure involved diluting ferritin catalyst (Sigma-Aldrich Co.) 40 times with de-ionized water. Then, the catalyst was spin cast onto degenerately doped Si substrates with a 100-nm-thick layer of thermal silicon dioxide dielectric. These wafers were heated to 900 °C to convert the ferritin to nanosized iron oxide particles.

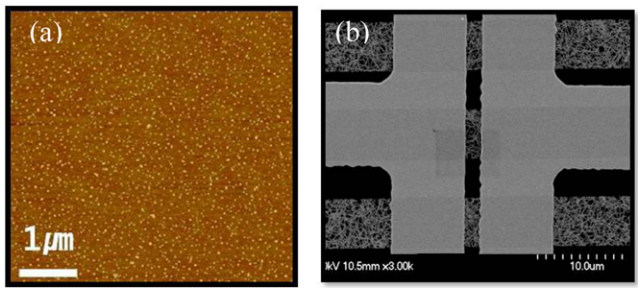

Fig. 1. (a) AFM image of Ferritin catalysts on the SiO_2/Si wafer after reduction. (b) SEM image of SWNT TFT after stripe patterning of the SWNT network and deposition of metal electrodes.

They were then cooled to room temperature in an air environment and then heated to 900 °C in hydrogen to reduce the catalyst to its active form. Fig. 1(a) shows the uniformly dispersed iron nanoparticles on the SiO_2/Si wafer after reduction. The height of the catalysts was 2-4 nm when measured with atomic force microscopy (AFM). SWNT growth was performed at 900 °C with CH_4 [500 SCCM (standard cubic centimeter per minute)] and H_2 (75 SCCM).

Reactive ion etching of the SWNTs using photolithographically defined patterns of resist was performed to create network stripes oriented along the transistor channels. These stripes prevent electrical crosstalk between devices [5]. To create the stripes, Shipley 1805 photoresist was spin-coated at 3,000 rpm onto the SWNT substrates. The photoresist was prebaked at 115 °C for 1 min, exposed to UV light for 6 s (120 mJ/cm^2) with a photomask that had 5-μm line and spacing patterns, and was then developed for 6 s in an MF-319 developer. After rinsing with de-ionized (DI) water and drying with nitrogen, these substrates were placed in a reactive ion etching (RIE) chamber (Plasma Therm 760) to etch the exposed SWNTs with O_2 plasma. Etching was done in a 20 SCCM O_2 flow at a pressure of 200 mTorr for 30 s at 100 W radio frequency power. Remaining

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photoresist was removed with acetone after the RIE treatment. SiO_2 and Si provided the gate dielectric and gate, respectively. The source and drain electrodes were formed using a conventional lift-off method with Ti(2 nm)/Au(40 nm). Fig. 1(b) shows the scanning electron microscopy (SEM) images of the final striped random network SWNT TFTs fabricated using the procedures described.

RESULTS AND DISCUSSION

1. Optimization of SWNT Growth

To optimize the growing conditions of SWNTs, the growing temperature, CH_4/H_2 ratio, in terms of the feed gas, catalyst concentration, and growing time, were varied. As can be seen in Fig. 2(a), when the growing temperature was varied, the highest tube density was obtained in the 850-900 °C temperature range. Tube densities were 21 tubes/μm^2 at 850 °C and 22 tubes/μm^2 at 900 °C, respectively, based on AFM measurements. Lower tube densities at lower growing temperatures can be explained by an effective reduction in carbon feed rate due to the slower rate of methane decomposition at lower temperature [19]. The decrease in tube density at 950 °C is due to the agglomeration of Fe catalyst particles.

To understand the effect of feed gas variations, the feed rate and ratio of CH_4 and H_2 were varied. As shown in Fig. 2(b), the highest tube density was obtained around H_2/CH_4=0.1 regardless of the total feed amount of CH_4. As Okita et al. reported, a small increase in the H_2 to CH_4 ratio keeps the size and activity of the catalyst particles small, as in the early stages of reaction, but excess H_2 results in larger size catalyst particles, and, therefore, suppresses the growth of SWNTs [20].

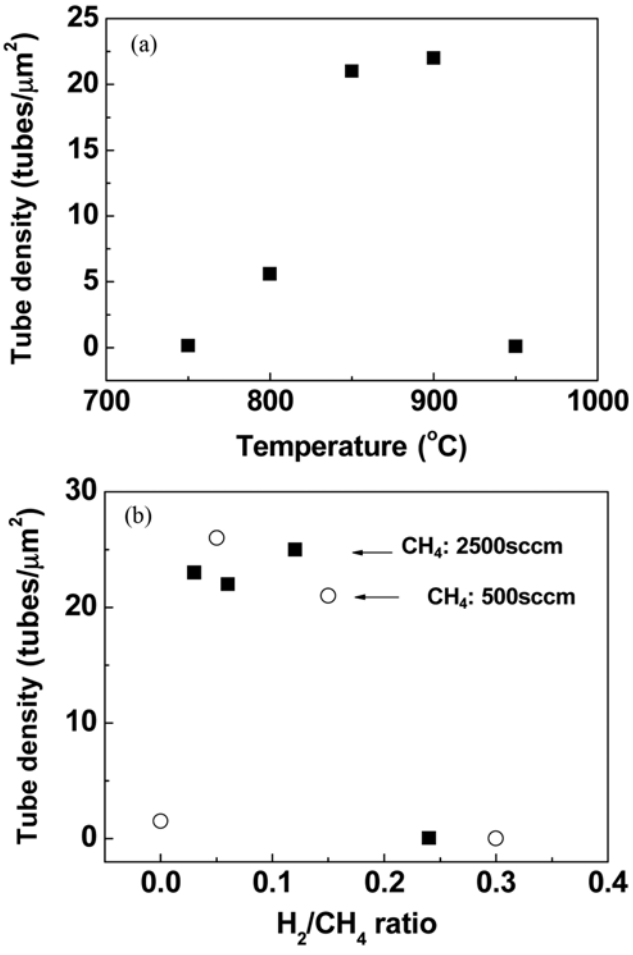

Fig. 2. (a) Tube density as a function of growth temperature, and (b) tube density as a function of the feed ratio of H_2 and CH_4.

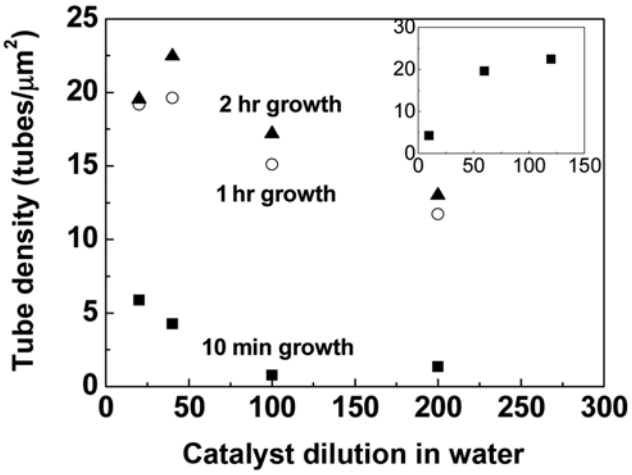

Fig. 3. Tube density as a function of catalyst concentration and growth time. Inset plot depicts the tube density as a function of growth time at 40 times catalyst dilution conditions (x axis: growing time, y axis: tube density in tubes/μm^2).

The tube density is also a function of the catalyst density and growing time. As shown in Fig. 3, as the catalyst density increases, the tube density increases except at 20 times dilution. Decreases in tube density at high catalyst concentration can be attributed to the agglomeration of Fe catalyst particles after reduction. The growth rate is fast initially and saturates after 60 minutes, as shown in the inset of Fig. 3. The saturation of the growth rate can be due to the viscous force of the hot surrounding gas that slows down SWNT growth [21,22]. In the early stages, the extrusive force is large enough to overcome the viscous force of the surrounding hot gas, but at steady state the equilibrium of the two forces results in slow and steady growth. After all of the growing conditions of SWNTs were optimized, SWNT TFTs were fabricated, and their hysteresis behavior was studied since the device mobility is linearly proportional to the tube density [11].

2. Hysteresis Behavior of SWNT TFTs on a SiO_2 Dielectric Layer

Fig. 4(a) and 4(b) show the hysteresis behavior of SWNT TFTs as functions of different gate sweep conditions and different TFT channel lengths. To compare the hysteresis behavior as a function of the TFT channel dimensions, both a long channel length (100 μm, Fig. 4(a)) device and short channel length device (2 μm, Fig. 4(b)) were tested. To compare the hysteresis behavior as a function of the gate sweep conditions, either the center voltage of the gate sweep was fixed (center Vgs=0, Fig. 4(a)), or the starting voltage of the gate sweep was fixed (start Vgs=−20 V, Fig. 4(b)).

The amount of hysteresis increases as the range of the gate sweep increases for both cases. Fig. 4(c), which provides a summary of results, shows that the amount of hysteresis is only proportional to the range of the gate sweep voltage and is independent of the TFT

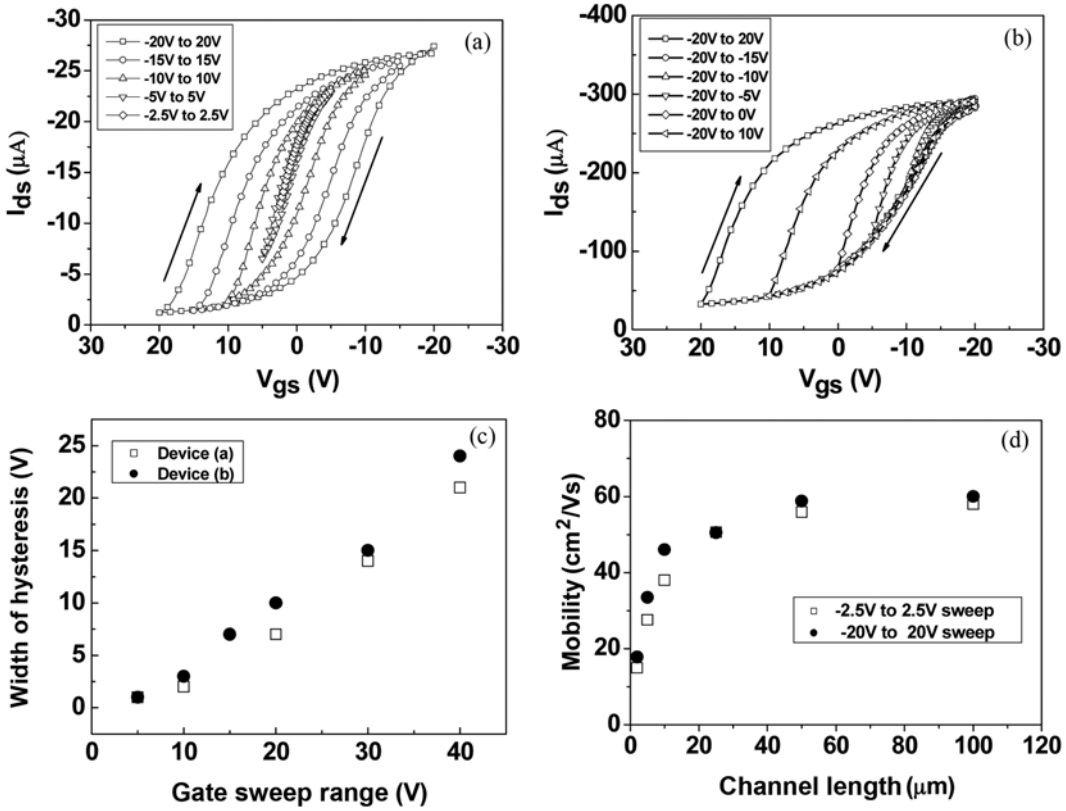

Fig. 4. Hysteresis behavior of SWNT TFTs as a function of the gate sweep condition and TFT channel dimension for (a) channel width (W): 250 μm, channel length (L): 100 μm, (b) W: 250 μm, L: 2 μm. The gate voltage was swept for a constant center voltage (a) and constant starting voltage (b). Arrows indicate the direction of the gate sweep. (c) Relation between the gate sweep range and the width of hysteresis, defined as the largest difference in gate voltage at the same Ids between forward and reverse gate voltage sweeps. (d) Comparison of mobilities of SWNT TFTs at different channel lengths and gate sweep ranges. For all cases, Vds was fixed at −0.5 V, and the channel width was 250 μm.

channel dimensions. Also, when the device mobilities were plotted against channel length, they were about the same for both the narrow range gate sweep (−2.5 V to 2.5 V) and the wide range gate sweep (−20 V to 20 V) at all tested channel lengths, as shown in Fig. 4(d). This suggests that the hysteresis does not change the intrinsic transport properties of SWNT TFTs and is only related to the charge exchange between the SWNTs and the dielectric layers.

To calculate the linear regime device mobility, the slope in the transfer characteristics was evaluated via the standard formula, mobility=$(\Delta Ids/\Delta Vgs)/(\varepsilon\varepsilon_0 VdsW/Lt)$, where Ids is the drain-source current, Vgs is the gate voltage, Vds is the drain-source voltage, t is the thickness of SiO_2 (100 nm), L is the channel length, ε is the dielectric constant of SiO_2 (3.9), ε_0 is the permittivity of free space, and W is the channel width [23]. The effects of fringing fields on the capacitance, which can be important at low network densities, were not considered. The physical width, W, of the channel was used for these computations.

To see the lifetime of injected charges, time measurement of the charge injection and relaxation was performed for the SWNT TFTs, as shown in Fig. 5. After applying a constant negative 20 V or positive 20 V to the gate for 1 minute at a constant Vds (0.5 V), the gate voltage was set to 0 V, and the drain-source current (Ids) was monitored for several minutes. Fig. 5 shows the relaxation results for the SWNT TFT after applying −20 V for 1 minute. The initial current

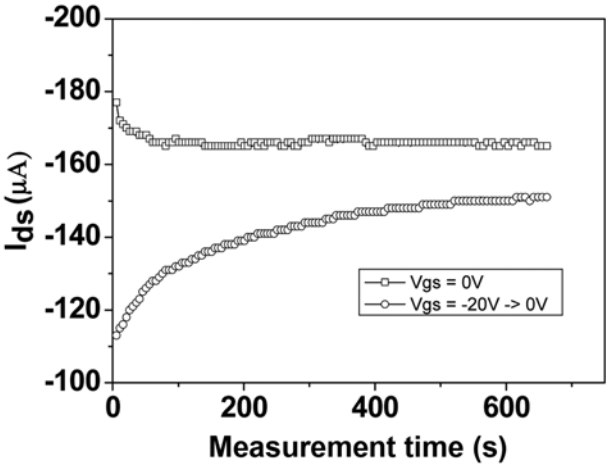

Fig. 5. Time measurement of drain-source current (Ids) measured at Vgs=0 V. The upper plot (-□-) was measured without charge injection, and the lower plot (-○-) was measured after 1 minute of charge injection with a −20 V gate bias. The channel length and channel width of the TFT were 2 μm and 250 μm, respectively.

drop can be attributed to the effective gate voltage change caused by positive charges injected from the SWNTs to the dielectric layer

[24]. The gradual increase in Ids indicates dissipation of the injected charges from the dielectric layer to ambient air or the SWNTs. Lifetimes of the injected charges were relatively long, and the Ids current had not recovered to the initial current at Vgs=0 V, even after 10 minutes of relaxation. This means that even after a long relaxation time the screening effect from the injected charges is still a factor. Since the measurement timespan of transfer characteristics that is generally used for SWNT TFTs is 1 minute, this long lifetime of injected charges is likely the main reason for the large hysteresis in the SWNT TFTs.

To determine the long lifetime effect of the injected charges, stepwise gate sweep tests were done with the same sweep ranges but with different sweep paths, and the results are shown in Fig. 6. As shown in Fig. 6(a) and (b), when the gate sweep follows a higher voltage→lower voltagevhigher voltage path (−20 V→−15 V→−20 V, or 20 V→15 V→20 V), there is almost no hysteresis; however, if the gate sweep follows a reverse path in the form lower voltage→higher voltage→lower voltage (−15 V→−20 V→−15 V, or 15 V→20 V→15 V), then the amount of hysteresis is the same as that of the full sweep condition. This result means that the behavior of the higher voltage→lower voltage→higher voltage path can be interpreted, as follows. Since a large amount of charges are injected by the absolute high gate voltage from the start, and their lifetime is long enough (such that they persist during the measurement), the effective gate voltage remains the same even if the device experiences a lower gate voltage, resulting in no hysteresis. However, for the lower voltage→higher voltage→lower voltage path, since the highest voltage is located in the middle of sweep, the effective gate voltage changes during the gate sweep so that there is a large hysteresis.

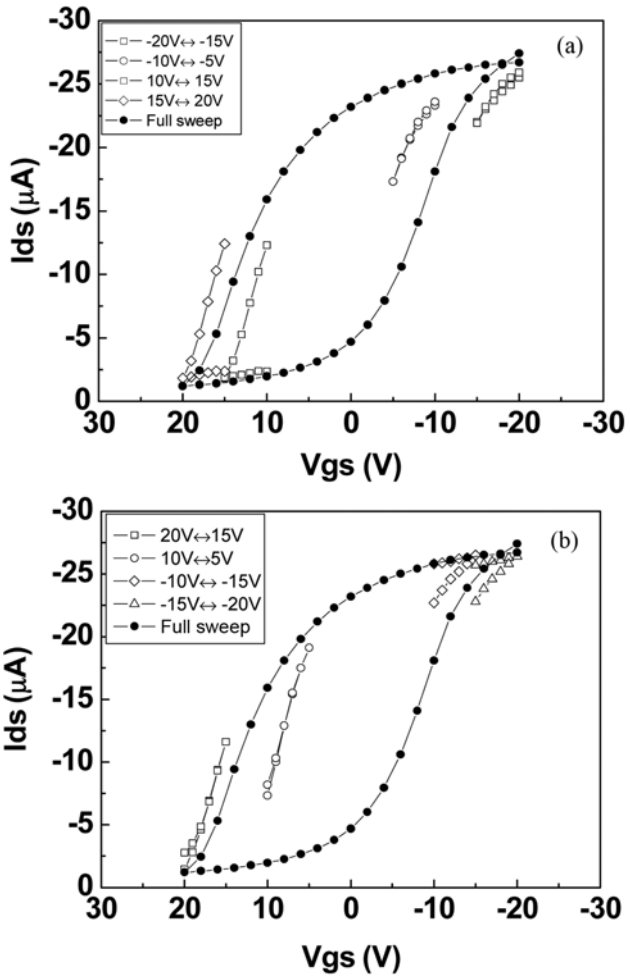

Fig. 6. Hysteresis behavior of SWNT TFTs as a function of the gate sweep path. (a) Gate sweep from lower voltage to higher voltage and return to lower voltage. (b) Gate sweep from higher voltage to lower voltage and return to higher voltage. The channel length and channel width of the TFT were 100 μm and 250 μm, respectively.

3. Reduction in the Hysteresis of SWNT TFTs with the SU-8 Top Gate

To determine the effect of the dielectric layer, a top gate SWNT TFT was fabricated, as described above. Fig. 7(a) provides an optical microscopic image of the fabricated top gate SWNT TFT. As shown in Fig. 7(b), the hysteresis behavior was the same before and

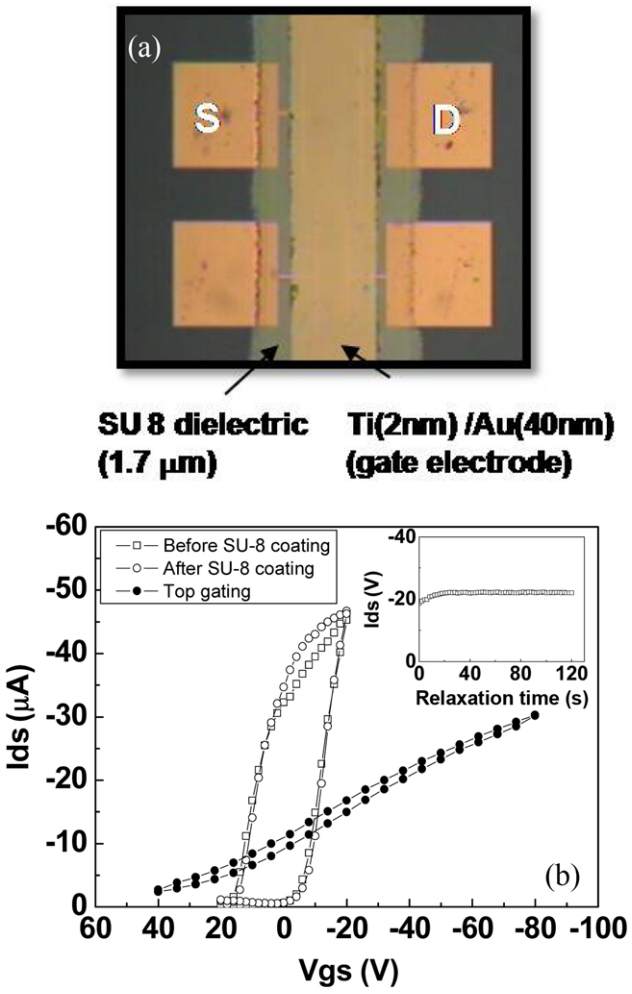

Fig. 7. (a) Optical image of the fabricated top gate SWNT TFT structure (b) Comparison of hysteresis behavior between the SU-8 (1.7 μm) based top gating and the SiO_2 (100 nm) based bottom gating for the SWNT TFT. The inset image shows time measurement of drain-source current (Ids) measured at Vgs=0 V after 1 minute charge injection with −80 V gate bias. The channel length and width were 100 μm and 250 μm, respectively.

after the SU-8 coating when the device was operated with the bottom gate, but the hysteresis was reduced significantly when the device was operated with the top gate. This reduced hysteresis was also shown in the time measurements, given in the Fig. 7(b) inset. This finding means that fewer charges were injected from the SWNTs to the SU-8 surface since SU-8 has hydrophobic surface properties [25], and there was no moisture on the surface of the SWNTs after SU-8 coating on top of the SWNT TFT channel. The calculated device mobilities were 26.9 cm^2/Vs for the bottom gating and 27.0 cm^2/Vs for the top gating, and, as shown, there was no change in the intrinsic properties of the SWNTs after SU-8 coating.

CONCLUSIONS

This paper shows that optimum temperature, feed composition, catalyst concentration, and growth time of SWNTs growth with Fe catalysts were 900 °C, H_2/CH_4=0.1, 40 times dilution with water, and 60 minutes, respectively. Furthermore, the hysteresis behavior of random network SWNT TFTs originated from the charge exchange between the SWNTs and dielectric layer rather than from a change in the intrinsic properties of the SWNTs, as shown by studying the gate sweep conditions and the SWNT TFT channel geometry. In addition, from the study of different gate sweep paths and the lifetimes of the injected charges, the long lifetime of the injected charges was another main reason for the huge hysteresis behavior observed in regular experiments. When the top gate SWNT TFTs were fabricated by using an SU-8 dielectric layer, the hysteresis was significantly reduced. This suggests a practical way to solve the hysteresis problem for applications of SWNT TFTs in electronic circuits.

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